REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the application.

Disposition of Claims

Claims 4, 16, and 27 are pending in the present application. Claims 4, 16, and 27 are independent.

Rejection(s) Under 35 U.S.C § 103

Claims 4, 16, and 27 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,043,672 ("Sugasawara"). For the reasons set forth below, this rejection is respectfully traversed.

Embodiments disclosed in this application are directed to a method and apparatus for fault analysis of integrated circuits. In accordance with one or more embodiments, an integral transient power supply current measuring unit measures a transient power supply current generated by a test pattern sequence outputted by a test pattern sequence input unit to take a time integral of the transient power supply current. The fault detector compares the time integral value measured by the measuring unit with a predetermined value to determine whether a delay fault is present or not in the analysis point of the circuit under test (*see* paragraph [0224] of the published specification). The analysis point may then be stored to correspond to the specific test pattern sequence used. Finally, a fault location generator may presume a fault location based on the analysis points associated with a given test pattern sequence that causes an abnormal power

supply current. Various examples of methods for presuming fault locations based on test pattern sequences may be found, for example, in paragraphs [0186]-[0204] of the specification.

Accordingly, claim 4 requires, in part, "presuming a fault location out of said analysis points based on said test pattern sequence, where the transient power supply current shows abnormality, and said analysis point stored to be corresponding to said test pattern sequence." Claims 16 and 27 each require analogous limitations. Advantageously, this feature of the claimed invention may enable users to find whether an electronic circuit has an open defect and short circuit current in an analysis point by simply inputting a specific test pattern sequence. Sugasawara fails to show or suggest at least the above discussed limitation with respect to claims 4, 16, and 27.

Sugasawara is directed to a test apparatus using selectable power supply lines for isolating defects in integrated circuits. Sugasawara suggests testing an IC based on quiescent current levels while a power supply line is divided into a plurality of parts. Specifically, Sugasawara teaches introducing dedicated power lines to each region of interest on an IC in order to isolate defects.

The Examiner asserts that Sugasawara suggests presuming a fault location, as required by claims 4, 16, and 27, on column 2, lines 49-53, which reads: "This approach has typically included measuring current in a region of the integrated circuit, cutting lines to sections within the same region other than the section of interest, and then taking additional measurements of current in the region." Applicant respectfully disagrees. The approach that Sugasawara discusses on column 4 merely suggests isolating various sections of an IC by cutting lines to other sections within the same region on the IC and measuring the quiescent currents. In fact, Sugasawara is completely silent with respect to the step of "presuming a fault location out

of said analysis points based on said test pattern sequence, where the transient power supply current shows abnormality, and said analysis point stored to be corresponding to said test pattern sequence," required by claims 4, 16, and 27. Further, there is no teaching that would render the above discussed limitation obvious in view of Sugasawara, because Sugasawara is completely silent with respect to the use of test pattern sequences to determine fault locations.

In view of the above, Sugasawara fails to disclose at least the above discussed limitation required by independent claims 4, 16, and 27. Further, there is no evidence that the above discussed limitation is obvious over Sugasawara. Claims 4, 16, and 27 are therefore patentable over Sugasawara. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 02008/071003).

Dated: 3/26/08

Respectfully submitted,

By _____

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